WHAT IS CLAIMED IS:

1. An integrated circuit in which a device for high-speed access, a device for low-speed access and a control circuit for controlling transfer of data to these devices are connected by a common bus in such a manner that transfer of data to the device for high-speed access takes priority, said integrated circuit comprising:

a switch circuit for performing control to turn on and off the bus connection between the device for high-speed access and the device for low-speed access; and

a control circuit for controlling said switch circuit so as to turn off the bus connection when data is transferred to the device for high-speed access and turn on the bus connection when data is transferred to the device for low-speed access.

2. The integrated circuit according to claim 1, wherein a plurality of devices inclusive of the device for high-speed access and the device for low-speed access are connected by the common bus so as to be given priority for data transfer in order of decreasing access speed;

said switch circuit being provided between mutually adjacent devices among said plurality of devices for turning on and off the bus connection between the mutually adjacent devices among said plurality of devices;

said control circuit controlling said switch circuits in sequence to turn on the bus connection so as

to make possible access to a device circuit having a higher access speed.

3. The integrated circuit according to claim 1, wherein the device for high-speed access, the device for low-speed access and the switch control circuit each operate in sync with clock pulses;

said integrated circuit further comprising a control circuit for outputting, in sync with the clock pulses, a data-transfer enable signal that enables transfer of data upon elapse of a fixed period of time after said control circuit controls said switch circuit so as to turn on the bus connection.

4. The integrated circuit according to claim 3, wherein output timing of the data-transfer enable signal output from said output circuit differs in dependence upon the access speeds of said devices.

5. The integrated circuit according to claim 3, wherein the period of the clock pulses varies in dependence upon the access speed of the device to be accessed.

6. A method of controlling an integrated circuit in which a device for high-speed access, a device for low-speed access and a control circuit for controlling transfer of data to these devices are connected by a common bus in such a manner that transfer of data to the device for high-speed access takes priority, said method comprising the steps of:

providing a switch circuit for performing control to turn on and off the bus connection between the device

for high-speed access and the device for low-speed access; and

controlling the switch circuit so as to turn off the bus connection when data is transferred to the device for high-speed access and turn on the bus connection when data is transferred to the device for low-speed access.